FAST National University of Computing and Emerging Sciences, Islamabad, Pakistan

ICD Integrated Circuit Design Lab

Design of a 4-Bit AC Nano-Processor for Self-Powered Biomedical and Smart Dust Applications

Ahsan Zia, Ajmal Khan, Ejaz Ahmed, Hadeesa Mehboob, Humbal Hammad, Junaid Razzaq, Muazam Iftikhar, Muhammad Arsalan, Shahrukh Hussain, Uzair Sharif, Dr.Hassan Saif, Dr. Khurram Javed, Dr. Rashad Ramzan

Project Scope:

Traditional Wireless Power Transfer (WPT) systems suffer from two key limitations: RF-to-DC rectifier inefficiency and large storage capacitor area requirements, hindering ultra-low-power applications like IoT nodes, biomedical implants, and wireless sensors.

Abstract:

A 4-bit AC nano-processor eliminates RF-to-DC rectifiers and large storage capacitors, enabling self-powered IoT nodes and smart dust. The AC logic family uses signal phase (0°/180°) for logic states and quadrature RF signals for timing control. Power and synchronization are derived directly from the RF field, supporting phase-domain computation. This enables reliable, long-term, battery-free operation in ultra-low-power applications.

Methodology:

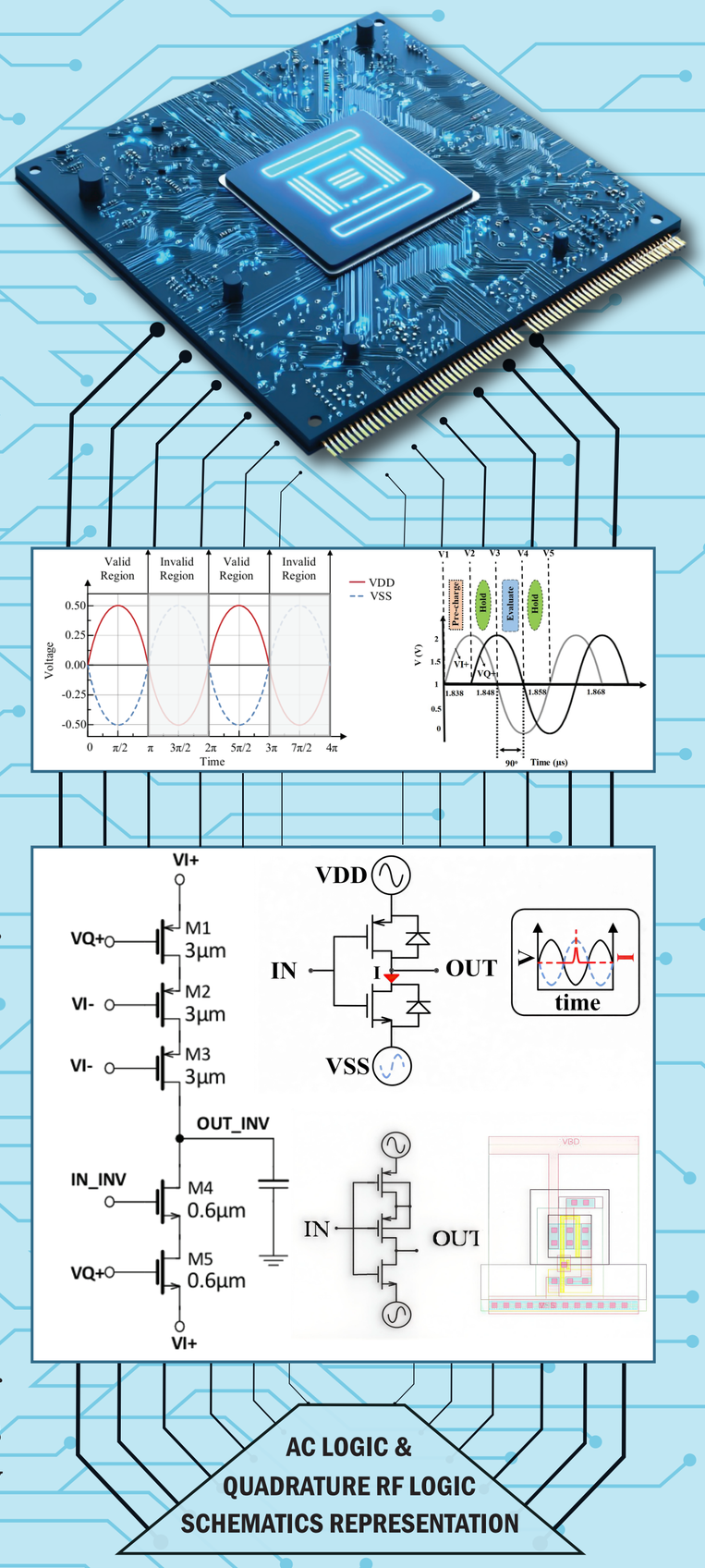
The methodology applies adiabatic CMOS logic to process sinusoidal signals with minimal power dissipation. Two approaches exploit phase differences between sinusoidal supplies: the first uses180° out-of-phase differential sinusoids, where their instantaneous voltage difference defines a valid logic evaluation region. The second employs 90° QRF signals to create distinct precharge, hold, and evaluation phases, enabling dynamic CMOS logic operation without requiring conventional DC supply generation.

Results:

Fundamental logic cells for both QRF-based and AC logic approaches have been designed and verified in 65 nm CMOS, including inverters, NAND, NOR, XOR, and DFF. The next step is integrating these validated cells into a fully functional 4-bit AC logic nano-processor to achieve improved system-level power efficiency using time-varying supply signals.

Future Work:

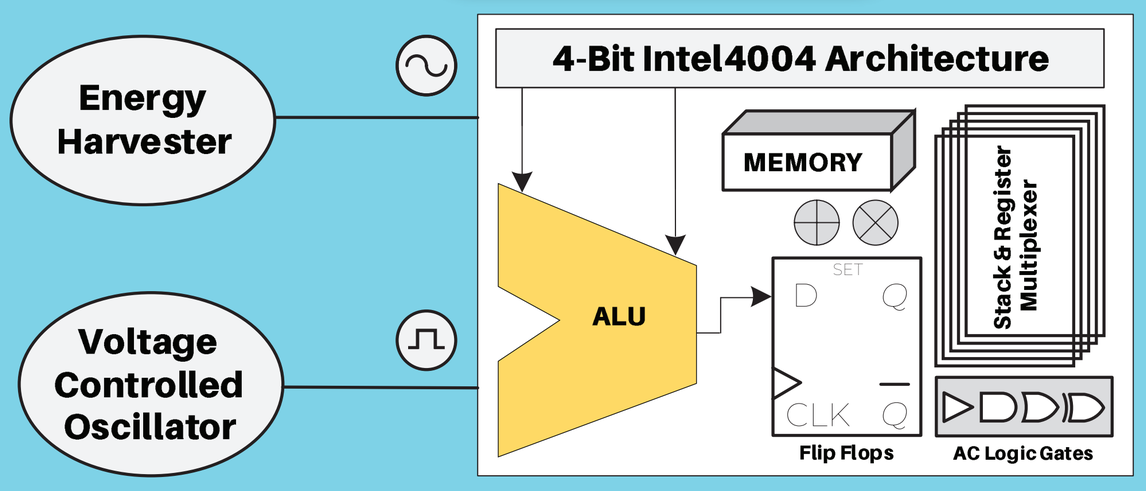
Future work involves integrating the validated logic cells into a complete 4-bit AC nano-processor for system-level evaluation. Physical fabrication and experimental validation of the rectifier-less architecture in 65 nm CMOS are planned. Further optimization for enhanced power efficiency and broader operating frequency range will also be explored.



COMPARISON TABLE

Aspect	AC Logic	Quadrature RF
Type	Two Sinusoids Signal 180° out of phase	Quadrature RF signals (I & Q) 90° apart
Topology	Static CMOS Structure (PUN + PDN)	Dynamic Logic Architecture
Regions	Valid, Invalid	Precharge, Hold, Evaluate
Isolation	Series PMOS with body-biasing technique	Double Isolation Transistor
Efficiency	53.9% Energy Saved at System Level	60% Less Power Consumption

FLOW DIAGRAM



SCAN NOW FOR MORE DETAILS